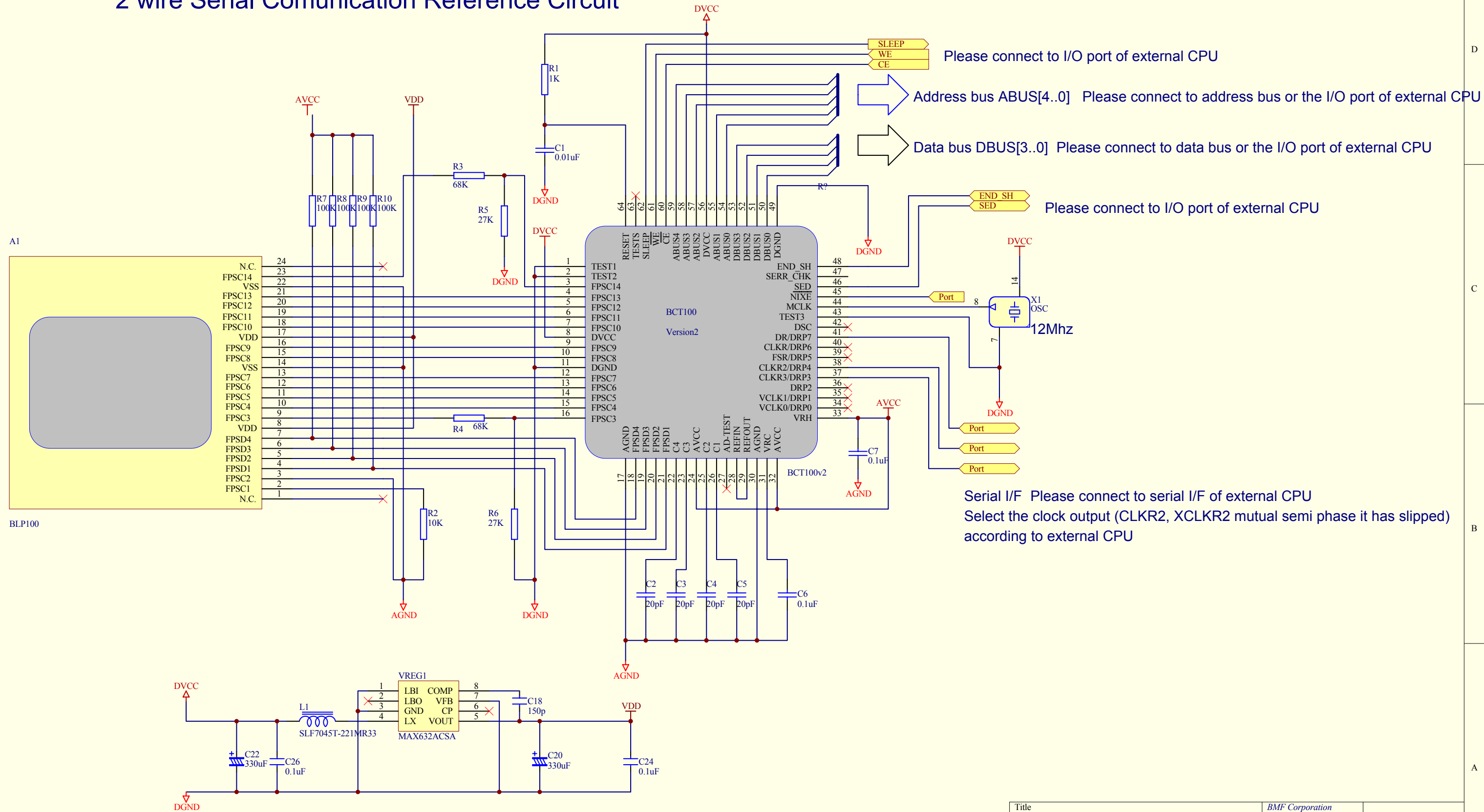


# 2 wire Serial Communication Reference Circuit



Please connect to I/O port of external CPU

Address bus ABUS[4..0] Please connect to address bus or the I/O port of external CPU

Data bus DBUS[3..0] Please connect to data bus or the I/O port of external CPU

Please connect to I/O port of external CPU

Serial I/F Please connect to serial I/F of external CPU  
 Select the clock output (CLKR2, XCLKR2 mutual semi phase it has slipped) according to external CPU